**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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| Applicant: | Priegnitz | Docket No: | TI-31455 |
| Serial No: | 09/768,504 | Examiner: | Laxton, Gary #22 |
| Filed: | 1/25/2001 | Art Unit: | 2838 |

For: ACTIVE GATE CLAMP FOR SELF DRIVEN SYNCHRONOUS RECTIFIERS



## APPEAL BRIEF PURSUANT TO 1.192(c)

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Tommie Chambers

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

The following Appeal Brief is respectfully submitted in triplicate and in connection with the above identified application in response to the final Office Action mailed August 12, 2003.

## REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated.

## RELATED APPEALS AND INTERFERENCES

Appellants legal representative knows of no appeals or interferences which will be directly affected, or have a bearing on the Board's decision.

## STATUS OF THE CLAIMS

Claims 1-15 were originally filed with Claim 16 being added. Thus, the subject matter of the instant appeal is the Final Rejection of Claims 1-16.

## STATUS OF AMENDMENTS

Claims 1-15 were originally filed. Claim 16 has been added. A Response After Final was filed on October 16, 2003.

## SUMMARY OF THE INVENTION

Referring to Figure 2, an input voltage 40, which 40 is supplied, for example, by a power supply unit of an electronic device, is provided at an input of a resonant primary snubber circuit including an inductor 42, capacitor 44 and diodes 46 and 48. These are connected to a primary side 50 of an isolation step-down transformer 52. A power switch in the form of a transistor 54 is also provided on the primary side 50.

On a secondary side 56 of the transformer 52, transistors 58 and 60 are shown. The gates of the transistors 58 and 60 are tied to a fixed voltage source 62. The secondary side 56 of the transformer 52 is also provided with rectifying transistors 64 and 66 as well as with a filter composed of an inductor 68 and a capacitor 70.

In operation, before the rectifier 66 turns on, its gate is at zero volts. The fixed voltage source 62 is typically 12 volts, so that the transistor 60 is fully enhanced. As a drain voltage is applied to the transistor 60, the gate of the rectifier 66 begins to charge. When the source of the transistor 60 and thus the gate of the rectifier 66 reaches about 10 volts, the transistor 60 turns off. This limits the peak voltage on the gate of the rectifier 66 to about 10 volts. The transistor 58 and rectifier 64 operate in a similar fashion.

Figure 3A and 3B show an exemplary embodiment of the present invention in an actual application.

Figure 4 is a simplified circuit diagram of a known flyback converter with self-driven synchronous rectifiers. A transformer 100 in the circuit is connected with the primary and secondary windings at opposite polarities. The circuit connected to the primary winding of the transformer 100 is in its most basic form a voltage supply 102 and a switch 104, shown here as a FET. A pulse 106 at a duty cycle as determined by a control (not shown) is provided at the gate, or control lead, of the switch 104.

The secondary side circuit of Figure 4 includes two FETs 108 and 110 connected for synchronous operation.

Figure 5, shows active gate clamp FETs 116 and 118.

In Figure 6 is shown a double-ended current doubler converter with self-driven rectifiers.

Figure 7 shows changes with respect to the circuit of Figure 6 in which active gate clamps 138 and 140 are provided for the synchronous FETs 128 and 130, respectively. The clamps 138 and 140 are FETs. A voltage source 142 is connected to the gates of the two clamps 138 and 140.

## ISSUES

The three issues on appeal are first whether Claims 1, 3, and 5-9 are unpatentable under 35 U.S.C. § 103 over Bowman in view of Shinada. Secondly, whether Claims 1-3, 5, 6, and 9-16 are unpatentable under 35 U.S.C. § 103 over Farrington in view of Shinada. And thirdly, whether Claims 7 and 8 are unpatentable under 35 U.S.C. § 103 over Farrington in combination with Bowman.

## GROUPING OF THE CLAIMS

Each of Claims 1 and 11 as contained in the attached Appendix are independently patentable, and these rejected claims do not stand or fall together for the reasons more clearly set forth herein below.

## ARGUMENTS

Bowman does not disclose or suggest the presently claimed invention including a voltage source connected to the first and second damping resistors to supply a fixed voltage to the control leads of the first and second transistors in the various forms in independent Claim 1, albeit a voltage through the damping resistors to the control leads of the first and second transistors in independent Claim 11.

Bowman discloses in Figure 15, rectifier switches 206 and 205 and gate drive switches 208 and 209.

Applicants agree with the examiner that Bowman does not disclose the first and second damping resistors.

Shinada does not disclose or suggest the presently claimed invention including the fixed voltage source connected to the first and second damping resistors to supply a voltage to the control leads of the first and second transistors in the various forms in independent Claims 1 and 11.

Shinada discloses impedance circuits 54 and 57 however; there is no mention of an applied voltage.

Farrington does not disclose or suggest the presently claimed invention including the fixed voltage source connected to the first and second damping resistors to supply

the voltage to the control leads of the first and second transistors in the various forms in independent Claims 1 and 11.

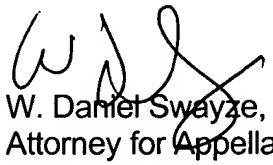
Applicants agree with the Examiner that Farrington does not disclose the first and second damping resistors.

## CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-16 under 35 U.S.C. § 103 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. **This form is submitted in triplicate.**

Respectfully submitted,



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## APPENDIX

1. A rectifier, comprising:

a reference primary circuit;

a transformer having a primary side connected to said reference primary circuit and having a secondary side;

first and second rectifiers in synchronous connection at said secondary side, said first and second rectifiers each having at least three leads, one of said three leads being a control lead;

first and second clamping transistors, said first clamping transistor being connected between said control lead of said first rectifier and said secondary side, said second clamping transistor being connected between said control lead of said second rectifier and said secondary side;

a first damping resistor connected to a control lead of said first clamping transistor and a second damping resistor connected to a control lead of said second clamping transistor;

a load connected to a same winding of said secondary side as said first and second clamping transistors; and

a fixed voltage source connected to said first and second damping resistors to supply a fixed voltage to said control leads of said first and second transistors.

2. A rectifier as claimed in Claim 1, wherein said secondary of said transformer has first and second leads, said first rectifier having first and second leads connected in series to said first lead of said secondary and said control lead connected to said

second lead of said secondary, said second rectifier having first and second leads across said first and second leads of said secondary and said control lead connected to said first lead of said secondary.

3. A rectifier as claimed in Claim 1, wherein said first and second rectifiers and said first and second clamping transistors are field effect transistors and said control leads are gate leads.

4. (Cancelled)

5. A rectifier as claimed in Claim 1, further comprising:

an output;

a first filter element connected between said first rectifier and said output; and

a second filter element connected between said output and ground.

6. A rectifier as claimed in Claim 5, wherein said first filter element includes an inductance and said second filter element includes a capacitance.

7. A rectifier as claimed in Claim 5, further comprising:

a third filter element connected between said second rectifier and ground.

8. A rectifier as claimed in Claim 7, wherein said first and third filter elements include an inductance.

9. A rectifier as claimed in Claim 1, wherein said transformer is connected with its windings at a same polarity.

10. A rectifier as claimed in Claim 1, wherein said transformer is connected with its windings at opposite polarity.

11. A self-driven synchronous rectifier, comprising:

a transformer having a primary and seconding winding;

an input for an input voltage connected to said primary winding;

a pair of rectifiers connected in a synchronous connection,

a first rectifier of said pair of rectifiers including a source drain connection in series with a first lead of said secondary winding and a gate connected to a second lead of said secondary winding;

a second rectifier of said pair of rectifiers having a source and drain leads connected across said first and second leads of said secondary winding and a gate connected to said first lead of said secondary winding;

a first transistor connected between said gate of said first rectifier and said second lead of said secondary winding;

a first damping resistor connected to a control lead of said first transistor;

a second transistor connected between said gate of said second rectifier and said first lead of said secondary winding;

a second damping resistor connected to a control lead of said second transistor;

a load connected to said secondary winding of said transformer; and

a voltage source connected to said first and second damping resistors to supply a voltage through said damping resistors to control leads of said first and second transistors.

12. A synchronous rectifier as claimed in Claim 11, further comprising:

a filter connected across said secondary winding of said transformer.

13. A synchronous rectifier as claimed in Claim 11, further comprising:

a resonate snubber connected across said primary winding of said transformer, said resonate snubber including a filter.

14. A synchronous rectifier as claimed in Claim 11, further comprising:

a switch connected at said primary winding of said transformer.

15. A synchronous rectifier as claimed in Claim 11, wherein said first and second transistors are field effect transistors and said control leads are gate leads.

16. A rectifier as claimed in Claim 2, wherein said control lead of said first rectifier is connected through said first clamping transistor to said second lead of said secondary;

said first lead of said second rectifier is connected to said first lead of said secondary through said first rectifier; and

said control lead of said second rectifier connected through said second clamping transistor to said first lead of said secondary.